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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/653,156
Filing Date ..... August 31, 2000
Inventor ..... Vishnu K. Agarwal, et al
Assignee..... Micron Technology, Inc.
Group Art Unit 2813
Examiner ..... Y. Huynh
Attorney's Docket No. MI22-1518
Title: Capacitor Fabrication Methods

RESPONSE TO MAY 10, 2002 OFFICE ACTION

To: Art Unit 2813
Assistant Commissioner for Patents
Washington, D.C. 20231

From: James E. Lake (Tel. 509-624-4276; Fax 509-838-3424)
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AMENDMENTS

In the Claims

Please replace claims 1, 7, and 10 with the following clean version of the amended claims, in accordance with 37 C.F.R. 1.121(c)(1)(i). Cancel all previous versions of any amended claim.

A marked up version showing amendments to any claims being changed is provided in one or more accompanying pages separate from this amendment in accordance with 37 C.F.R. 1.121(c)(1)(ii). Any claim not accompanied by a marked up version has not been changed relative to the immediate prior version, except that marked up versions are not being supplied for any added claim or canceled claim.

1. (twice amended) A capacitor fabrication method comprising:

forming a first capacitor electrode comprising TiN over a substrate, the first electrode having an innermost surface area per unit area and an outermost surface area per unit area that are both greater than an outer surface area per unit area of the substrate;

forming a capacitor dielectric layer over the first electrode; and

forming a second capacitor electrode over the dielectric layer.

7. (once amended) The method of claim 1 wherein the outermost surface area of the first electrode is at least 30% greater than the outer surface area of the substrate.

10. (once amended) A capacitor fabrication method comprising:

forming an opening in an insulative layer over a substrate, the opening having sides and a bottom;

forming a layer of polysilicon over the sides and bottom of the opening;

removing the polysilicon layer from over the bottom of the opening;

converting at least some of the polysilicon layer to hemispherical grain polysilicon;

conformally forming a first capacitor electrode on the hemispherical grain polysilicon, the first electrode being sufficiently thin that the first electrode has an outermost surface area per unit area greater than an outer surface area per unit area of the substrate underlying the first electrode;

forming a capacitor dielectric layer on the first electrode; and

forming a second capacitor electrode over the dielectric layer.